Ammonia-source molecular beam epitaxy of ScAlN/GaN heterostructures for high-power high-frequency applications

C. Elias, S. Chenot, M. Nemoz, F. Bartoli, A. Courville,

V. Gallardo Mödinger, P. Vennéguès, M. Hugues, Y. Cordier*

[1]Université Côte d'Azur, CNRS, CRHEA, Valbonne, FRANCE

*yvon.cordier@crhea.cnrs.fr

ScAlN is a wide bandgap semiconductor with large piezoelectric and spontaneous polarization coefficients ensuring a very high charge density at the interface with GaN, which makes it a promising barrier layer for HEMTs in view of power switching and RF/mm-wave power amplifier applications. Furthermore, it can benefit ferroelectric properties opening the way for new applications. The development of the epitaxy of this alloy has started with plasma-assisted MBE, followed by MOVPE. More recently, we have demonstrated the feasibility of the growth with ammonia source MBE under nitrogen-rich regime and an optimum temperature was identified for the growth of $Sc_xAl_{1-x}N$ barriers quasi-lattice matched on GaN (x~14%) [1]. The advantages of this growth regime in terms of growth rate, alloy composition and homogeneity [2] have been demonstrated. HEMT heterostructures have been grown on GaN-on-Si and GaN-on-Sapphire templates, demonstrating two-dimensional electron gases (2DEGs) with charge densities Ns-cv ranging from $2x10^{13}$ to $4x10^{13}/cm^2$ depending on the nominal thickness of the ScAlN barrier which was varied from 5 nm to 25 nm. Functional transistors with 9 µm source-drain spacing have been fabricated on these heterostructures. Drain current density exceeds 700 mA/mm on 10 nm barrier and 1 A/mm on 25 nm barrier (twice the one obtained on our standard AlGaN/GaN devices) while a limited gate leakage current could be observed up to a drain voltage of 100 V. This result is of primary importance as the gate leakage through the ScAlN barrier has been reported as a major concern [3]. However, the surface of ScAlN rapidly oxidizes and suffers a lack of stability during the device process. For this reason, in-situ grown cap layers such as GaN and AlN have been studied. According to Hall effect measurements, the room-temperature electron mobility in the 2DEG of most of the samples ranges from 500 to about 1000 $cm^2/V.s$ depending on the quality of the interface between ScAlN and GaN which features a 1-2 nm AlN exclusion layer. The typical 2DEG sheet resistances range between 240 and 300 Ohm/sq. In absence of the AlN exclusion layer, the resistance rises to 785 ohm/sq. Furthermore, optimizations of the growth of a 10 nm barrier HEMT lead to a sheet resistance of 210 ohm/sq, a promising result for the fabrication of high-performance transistors.

This work is partly supported by the French technology facility network RENATECH, the French National Research Agency (ANR) through the 'Investissements d'Avenir' program GaNeX (ANR-11-LABX-0014 and the project TWINS (ANR-23-CE51-0011) as well as ECSEL JU project GaN4AP under Grant Agreement No. 101007310.

[1] C. Elias et al, Appl. Phys. Lett. Materials 11, 031105 (2023).
[2] S. Ndiaye et al, Appl. Phys. Lett. 123, 162102 (2023).
[3] P. Döring et al, Appl. Phys. Lett. 123, 032101 (2023).

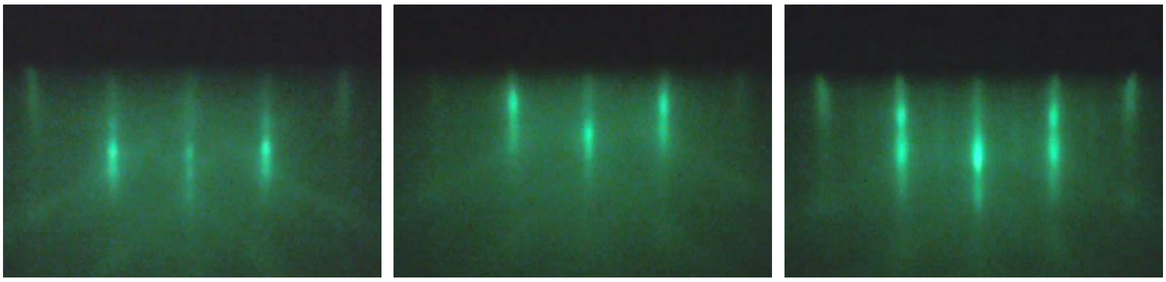

Fig. 1: RHEED patterns of the surface of ScAlN (left) capped with AlN (centre) or GaN (right).

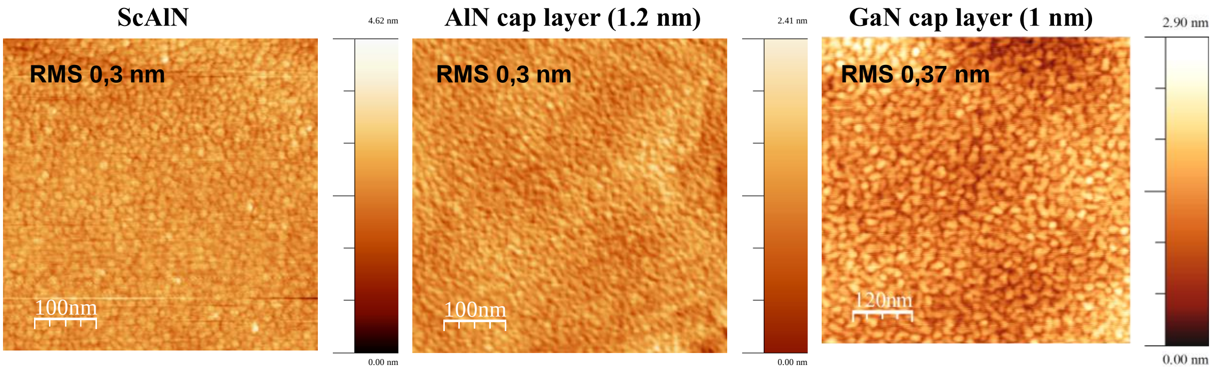

Fig. 2: Tapping mode atomic force microscopy images showing the morphology of ScAlN (left) capped with AlN (centre) or GaN (right).

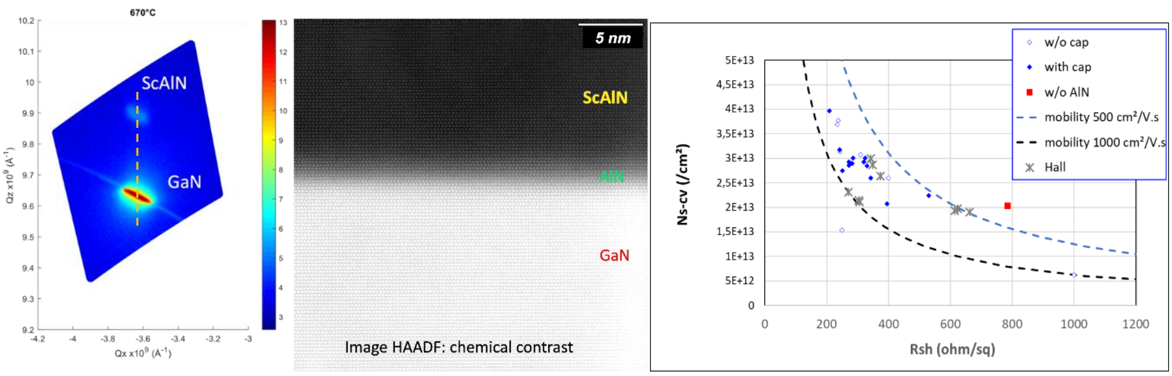

Fig. 3: Left: X-ray diffraction reciprocal space map around the (10$\bar{1}$5) node showing the in-plane lattice matching of ScAlN with GaN. Centre: high-resolution cross-section transmission electron microscopy view of the HEMT interface. Right: transport properties of the ScAlN/GaN HEMTs.

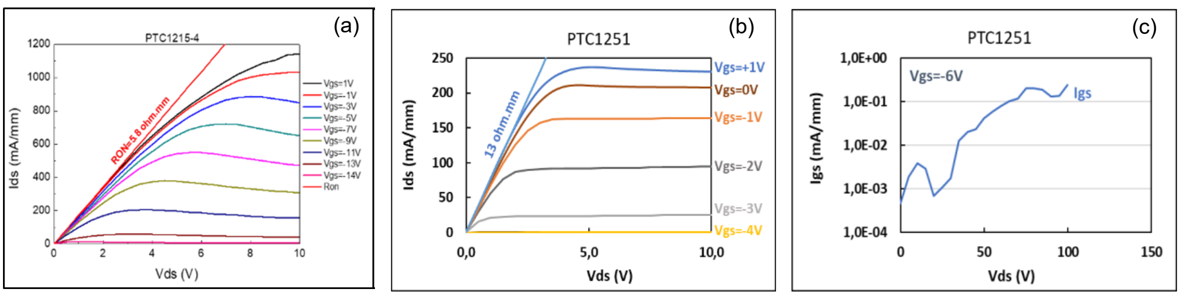

Fig. **4**: DC output characteristics Ids(Vds,Vgs) of 2 µm gate transistors with 9 µm source-drain spacing fabricated on the ScAlN/GaN HEMT grown on Silicon with (a) a 25 nm barrier and (b) a 10 nm barrier. (c) Gate leakage of the 10 nm barrier HEMT in 3-terminal off-state configuration.