Bottom gated in-plane selective area grown InSb nanowires on GaAs(111)B

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The selective area growth (SAG) of a semiconductor inside a dielectric mask fabricated by e-beam lithography enables the design of in-plane nanostructures with an arbitrary shape and a deterministic position. This scalable process applied to strong spin-orbit semiconductors such as InSb or InAs is very interesting for the fabrication of quantum devices involving branched NW or nano-resonators exploiting coherent electron transport [1, 2]. However, in this configuration, tuning the charge density in the NW is generally achieved with a top gate, limiting the possibility to adjust the Fermi level inside semiconductor/superconductor hybrid nanostructures that aim to demonstrate Majorana Zero mode [2]. In this work, we investigate (i) the growth of in-plane InSb NWs on a GaAs(111) substrate by atomic hydrogen assisted Selective Area Molecular Beam Epitaxy (SAMBE) and (ii) the possibility to tune the charge density and the conductivity inside the NW by adding a GaInP top barrier on the substrate before the mask fabrication.

An InSb thin film is first grown on a 100 nm $Ga_{0.5}In_{0.5}P$ barrier deposited on a n-doped ($n=3\times 10^{18}$ cm^{-3}) GaAs $(111)_B$ substrate (figure 1a). To ensure a quasi-two dimensional growth of InSb despite the 14.6% lattice mismatch between InSb and GaAs, a very large Sb/In flux ratio of 120 is used. As shown in figure 1b, a quite smooth surface with a low density of nano-holes is achieved after a 100nm-thick InSb growth. After processing Van der Pauw and TLM devices from this layer, we measure a 300K Hall mobility of 11000$cm^2.V^{-1}.s^{-1}$ and evidence an efficient command of the source-drain current with the bottom gate. We used the same growth conditions for the SAMBE of InSb NWs on patterned GaInP/GaAs:n+ substrates (figure 2a). Scanning Electron Microscopy reveals that quite good morphology can be obtained for the NWs (figure 2b) after 50 nm deposition. Using Transmission Electron Microscopy, we evidence that most of the mismatched between InSb and GaInP is accommodated with an array of misfit dislocations at the interface together with some stacking faults within the InSb nanostructures. A variation of the resistance of 100nm-wide NWs with bottom gate bias is demonstrated using 4P-STM measurements at room temperature (figure 2d). More details about the structure of the NWs and their electrical measurements will be given during the conference.

Acknowledgments and References

This study was financially supported by the French National Research agency under the program Equipex EXCELSIOR, INSPIRING ANR project (ANR-21-CE09-0026-01), PHC PROCOPE project (N°50795SA), the French Technological Network Renatech, and the Région Hauts de France.

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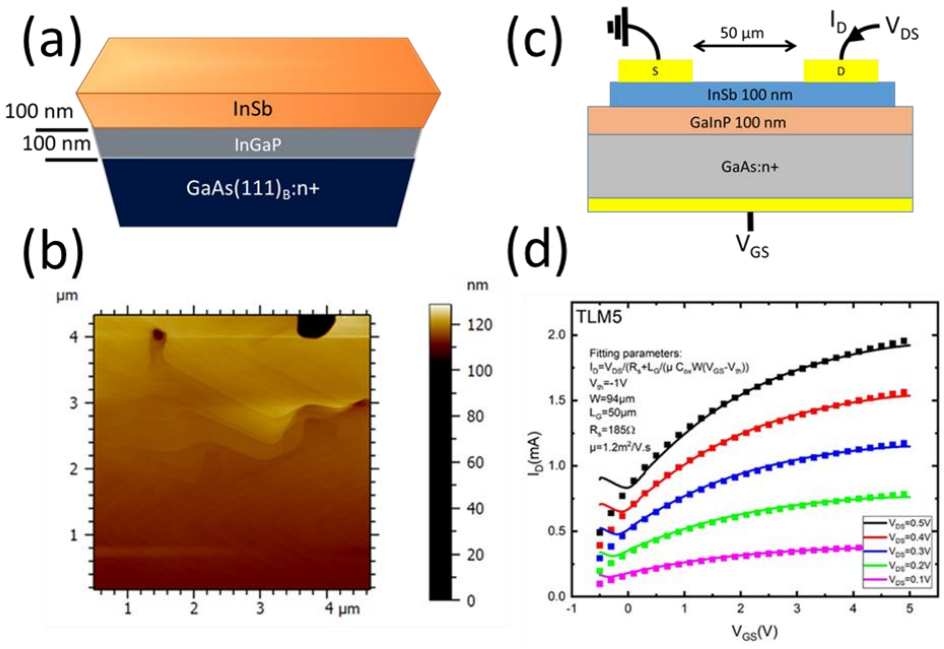

Fig. 1: Structure of the stack of two dimensional InSb/GaInP/GaAs sample (a). AFM image of the surface of the sample (b), Schematics of the device used for the transfer measurements displayed in (d) for different drain voltage. Solid line corresponds to the measurements and dot line to the fit.

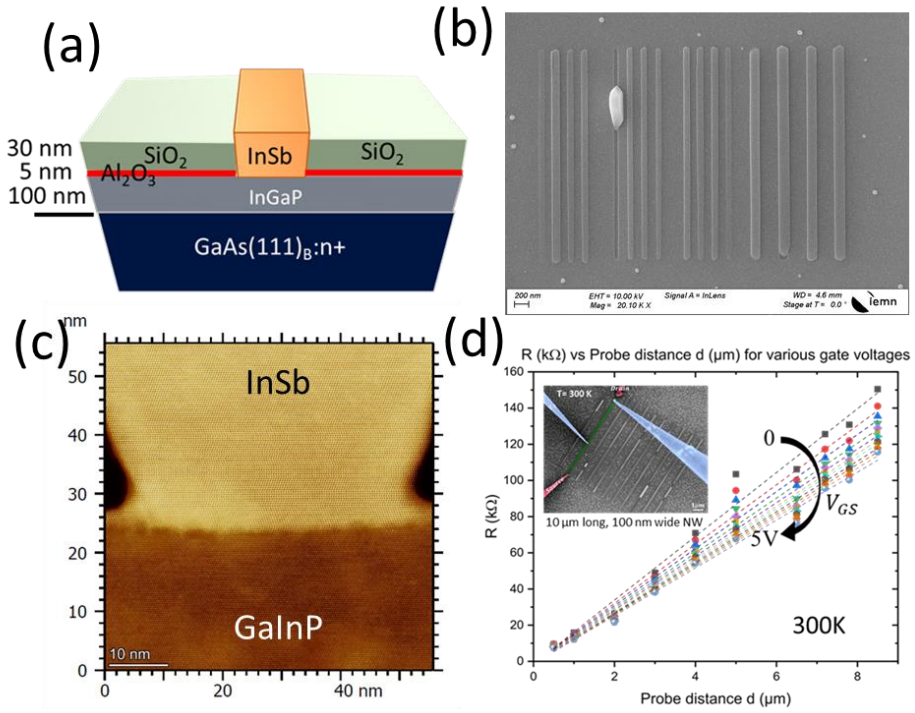

Fig. 2: Structure of the NWs grown by SAMBE (a). SEM image of an array of NWs after 50 nm deposition (b). Cross section TEM image of the interface between InSb NW and GaInP buffer layer (c). Resistance of the NW versus the inner probe distance measured on single 100nm wide InSb NW.